REMARKS

The Examiner's Action mailed on June 29, 2005 has been received and its contents carefully considered. In this Amendment, claims 1 and 5 have been amended. Claims 1-7 are now pending in the application. Fig. 2A is amended to correct the informalities. The specification and abstract are also amended, to correct grammatical errors, improve the idiomatic English, provide better clarify and overcome the specific objections set forth by the Examiner. No new matter is introduced by any of these amendments. For at least the following reasons, it is submitted that this application is in condition for allowance.

The Examiner has objected the drawing Fig. 2A and specification as containing informalities. The drawing Fig. 2A and the specification have been amended accordingly. The objections therefore no longer are applicable and accordingly to be withdrawn.

Claims 1 and 5 are rejected under 35 U.S.C. 112 as being indefinite for lack of proper antecedent basis. Claims 1 and 5 are amended to assure such basis, and it is respectfully submitted that the rejection is no longer applicable and accordingly should be withdrawn.

Claims 1 and 4-7 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Sato* (U.S. Patent No. 6,665,268) in view of *Heller* (U.S. Patent 4,907,230). However, independent claims 1 and 5 has been amended for improved clarity, and it is submitted that amended claims 1 and 5 are patentable over *Sato* in view of *Heller* for at least the following reasons:

(1) It would not be obvious to a person skilled in the art to look to the *Sato* and *Heller* references to solve the problems of the invention, and it would not be obvious to combine the teachings of the references in the manner suggested; and

(2) Even if the references were combined, the claimed invention would not be obtained.

1. Nonobviousness of applying the references

First addressing the rejection of claim 1, it is noted that amended claim 1 recites:

"A method for performing a load flow test **among a plurality of IEEE 1394 controllers**, wherein **said IEEE 1394 controllers are disposed on a plurality of interface cards individually**, said method comprising the steps of:

(a) initializing said interface cards and setting one of said interface card as a master interface card and the other interface cards as slave interface cards;

(b) said master interface card initializing a plurality of communication protocol packets while said slave interface cards sending a plurality of first ready signals;

(c) said master interface card sending said communication protocol packets to the slave interface cards **for responding to said first ready signals**;

(d) said slave interface card sending a plurality of second ready signals for responding to the communication protocol packets sent by said master interface card;

(e) said master interface card starting to **perform said load flow test** for responding to the second ready signals;

(f) checking status of every interface card for confirming whether an error occurs or not and sending a plurality of check packets to the slave interface cards by said master interface card, wherein debugging is performed if said error occurs;

(g) said slave interface cards sending a plurality of third ready signal for responding to the check packets;

(h) said master interface card sending a plurality of confirm signals to said slave interface cards for responding to said third ready signals; and

(i) said slave interface cards checking said test results for responding to said confirm signals;

wherein steps (a) to (i) are performed sequentially"
(where text is bolded for emphasis and underlined to indicate an added limitation.

Sato discloses:

> "FIG. 1 is a block diagram showing a configuration according to a first embodiment of the present invention. A crossbar network unit 10 and processor elements PE_0 to PE_3 making up a **parallel processor system** are shown in FIG. 1. A load testing apparatus according to the first embodiment described below is for conducting a **load test on this parallel processor system**. **The parallel processor system** is a kind of **supercomputer** for realizing a super high-speed arithmetic operation by causing the processor elements PE_0 to PE_3 to execute the parallel processing."

(See col. 11, lines 49-58)

Sato also discloses:

> "In FIG. 1, the processor elements PE_0 to PE_3 are arithmetic elements for executing the parallel arithmetic operations in accordance with a parallel algorithm and each include a CPU, a memory, etc."

(See col. 11, lines 59-62)

It is noted that *Sato* discloses that a load testing apparatus is for conducting a load test on a parallel processor system, which is a kind of supercomputer. The parallel processor system comprises several processor elements each of which includes a CPU, a memory, etc. Because an interface card is used for connecting a peripheral device to a processor element, it is apparent that the interface card operates in quite a different way than the processor element operates. Therefore, *Sato's* method is performed in a very different technical field to solve a different problem than that of the invention, that is, *Sato's* method is not in an analogous art.

Further, *Heller* discloses:

"Another object of the invention is to detect faults in PCB's at the component level, while the components are in-circuit, without damage to the component.

Another object of the invention is to provide a tester that will test functionally at the board level and at the component level while the components are in-circuit. The invention detects open circuits and short circuits among components. The invention also tests analog and digital components at the component level. It tests IC's for open inputs, pins pulled to the power supply or to ground, and for shorts between inputs and outputs, and for internal IC failures (emphasis added),."

(See col. 5, lines 29-41)

Heller's object is "to detect faults in PCB's at the component level, while the components are in-circuit" and "to provide a tester that will test functionally at the board level and at the component level while the components are in-circuit" (emphasis added), Therefore, *Heller's* is from a very different technical field than that of the invention or *Sato's* method. Nor is *Heller's* method in an art analogous to the invention,.

Because *Sato*'s and *Heller's* methods are in different and nonanalogous technical fields, it would not have been obvious of to a person having ordinary skill in the art the time the invention was made to combine the the teachings *Sato*'s and *Heller*'s methods to obtain the invention defined by amended claim 1. Therefore, the invention defined by claim 1 is clearly unobvious under 35 USC 103(a).

2. The teachings of the references, even when combined, do not produce the claimed invention

Moreover, even of the teachings in *Sato*'s and *Heller's* disclosures are combined, the combination does not provide or suggest the invention defined by amended claim 1.

The Examiner apparently regards step (c) of amended claim 1 as corresponding to steps SI4 and SI5 in *Sato*'s Fig. 27. However, *Sato* disclose "in step SI3, the processor element PE_A (master program) determines whether the test information (including packets) shown in FIG. 25 is to be transmitted or not to the processor elements PE_B to PE_E (slave programs) through the service processor 60 shown in FIG. 22"; (Col. 47, lines 13-17) and "in the case where the determination in step SI3 is YES, the processor element PE_A (master program) proceeds to step SI5." (See col. 47, lines 20-22) The steps SI4 and SI5 are performed when the test information (including packets) shown in FIG. 25 is to be transmitted to or not to be transmitted to the processor elements PE_B to PE_E respectively. The steps SI4 and SI5 are performed not for responding to the first ready signals, which are sent by said slave interface cards, as recited in steps (b) and (c) of amended claim 1. Therefore, *Sato* does not disclose the step (c): "said master interface card sending said communication protocol packets to the slave interface cards for responding to said first ready signals".

The Examiner apparently regards step (e) of amended claim 1 as corresponding to step SI7 in *Sato*'s Fig. 27. *Sato* discloses "in step SI7, the processor element PE_A transmits the packet of packet ID 0 shown in FIG. 25 to the destination processor element PE_A, and then proceeds to step SI8, where it is determined whether a fault is detected at the time of transmission or not. In the case where this determination is NO, the process proceeds to step SI9." (See col. 47, lines 50-55) However, in *Sato*'s step SI7, only the packet of packet ID 0 is transmitted to the processor element PE_A. *Sato*'s

Step SI7 does not disclose step (e) "said master interface card starting to perform said load flow test for responding to the second ready signals".

The Examiner also appears to regard part of the step (f) in amended claim 1 as corresponding to steps SI31-33 in *Sato*'s Fig. 27. However, what is performed before *Sato*'s steps SI31-SI33 is *Sato*'s step SI30, not *Sato*'s step SI7, which is regarded as corresponding to step (e) in claim 1. Therefore, *Sato* does not disclose that step (f) follows step (e) as recited in amended claim 1.

The Examiner regard the step (g) in amended claim 1 as steps SI33-YES in *Sato*'s Fig. 27. However, only whether "received packet legitimate one" is determined in *Sato*'s step SI33. The step SI33 does not disclose "said slave interface cards sending a plurality of third ready signal for responding to the check packets" as recited in the step (g) of amended claim 1.

The Examiner regard the step (h) in amended claim 1 as steps SI14-YES in *Sato*'s Fig. 27. However, what performed before *Sato*'s steps SI14 is *Sato*'s step SI13, not *Sato*'s step SI33-YES, which is regarded as the step (g) in claim 1. Therefore, *Sato* does not disclose that step (h) follows step (g) as recited in claim 1.

Since features recited in amended claim 1 are not disclosed by *Sato* and *Heller*, it would not have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of *Sato* in view of *Heller*. In view of the above, it is respectfully submitted that the rejection under 35 USC103(a) should be withdrawn.

As such, it is submitted that claims 2-4, which depend from claim 1, also clearly are patentable over *Sato* and *Heller*. Moreover, since claim 5 has been amended similarly to the amendment of claim 1, therefore, for reasons similar to those presented above as to the patentability of claims 1-4, the rejection of claims 5-7 under 103(a) also should be withdrawn. Therefore, based on the above it is submitted that the application is in condition for allowance and such a Notice, with allowed claims 1-7 earnestly is solicited.

If the Examiner believes that a conference would be of value in expediting the prosecution of this application, the Examiner is hereby invited to telephone the undersigned counsel to arrange for such a conference.

Respectfully submitted,

October 28, 2005
Date

Steven M. Rabin - Reg. No. 29,102
RABIN & BERDO, P.C.
Telephone: (202) 371-8976
Telefax: (202) 408-0924
CUSTOMER NO. 23995

SMR:pjl

Amendments to the Drawings

Please replace Fig. 2A with the attached amended Fig. 2A. The informalities in this drawing, which are recited in the Examiner's Action are corrected accordingly, as well as to correct grammatical errors in steps 215, 225 and 230.